



Investor Presentation

August 2018



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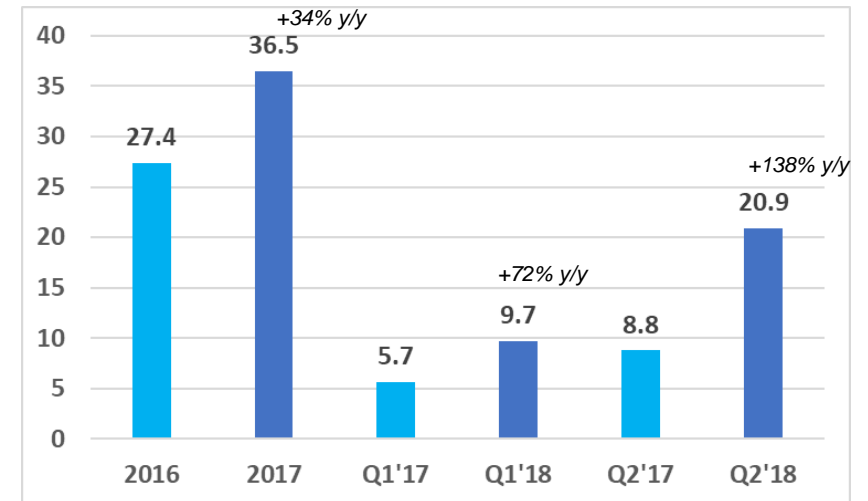
Unless the context requires otherwise, references to “ACM,” “we” and “our” refer to ACM Research, Inc. and its subsidiaries.

ACM Research Highlights

Company Background

- ACM Research, Inc. (NASDAQ: ACMR) develops and manufactures **best-in-class** cleaning tools to drive higher yields for advanced production nodes and geometries
- Patented **megasonic technology** delivers highly effective single-wafer wet cleaning for flat and simple structures (SAPS), and damage-free cleaning for advanced 3D patterned wafers (TEBO)
- HQ in Fremont, CA with operations in Shanghai, China and more than 250 employees. **193 patents** granted in the U.S., PRC, Japan, Korea, Singapore and Taiwan (as of 5/15/2018)
- Highly referenceable **customers and in-region support** position ACM to scale business with China's investment cycle
- Products address an estimated **55% of the \$2.7B** Single Wafer Cleaning Market, with future expansion from new products
- Recent capacity expansion provides the floor-space to support more than **\$350 million** of annual production

ACM Annual & YTD Revenue Comparison (\$M)



World Class Customer Base

Advanced Cleaning Tools



YMTC



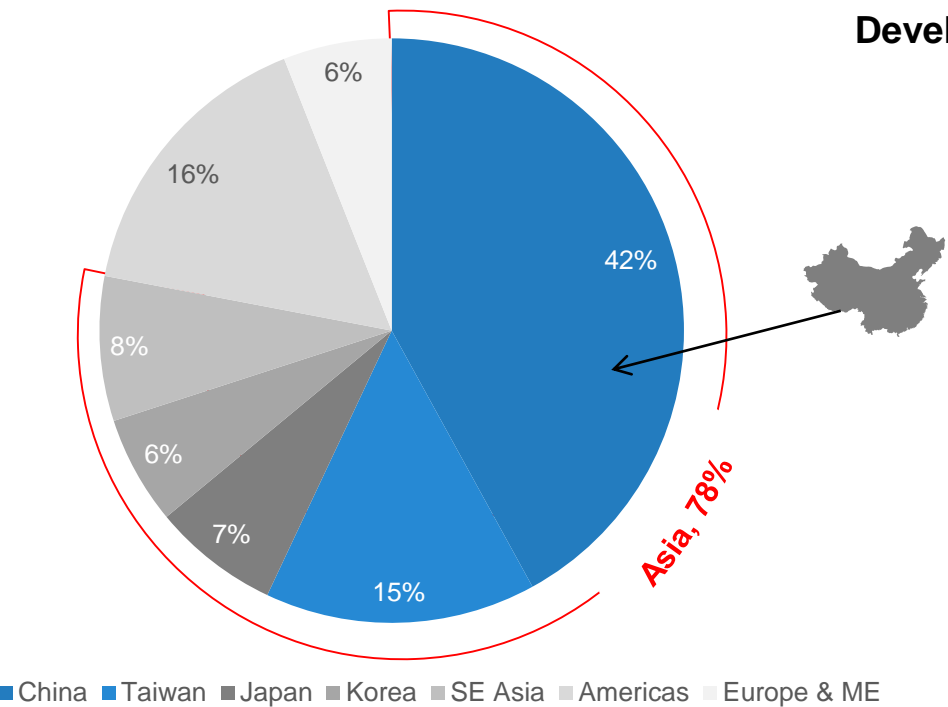
China DRAM J.V.

Advanced Wafer-Level Packaging & Mfg Tools



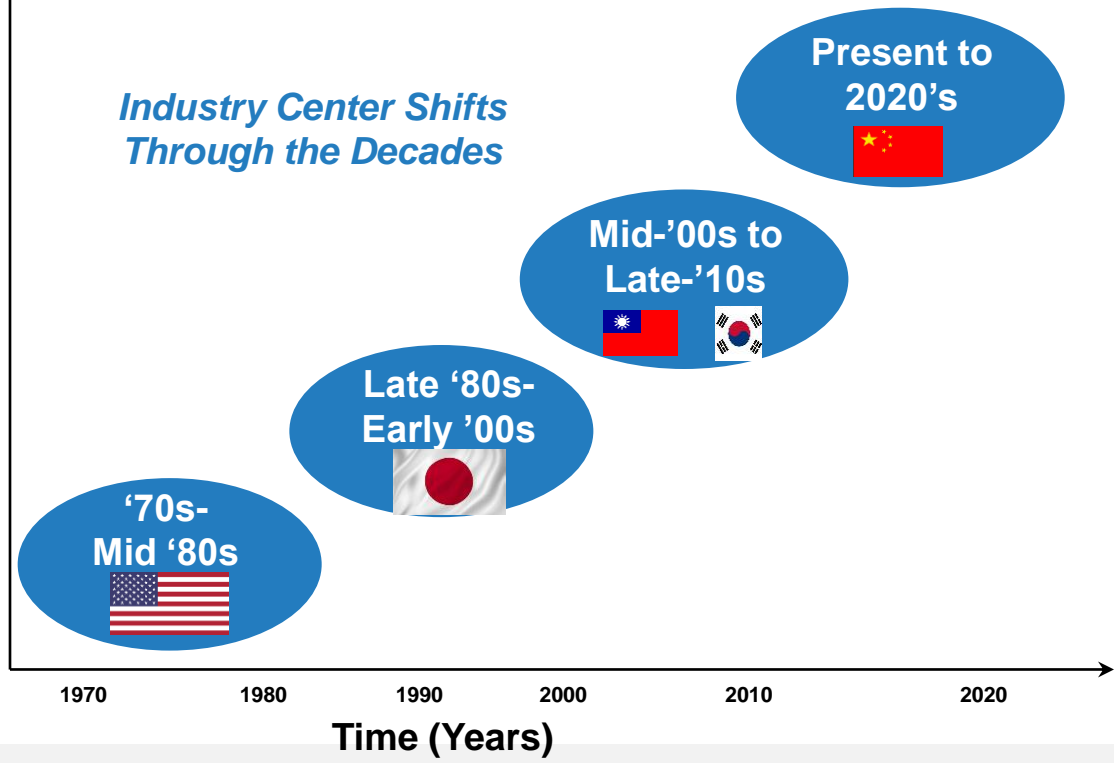
ACM Well-Positioned to Participate in Asia Fab Investments

New Facilities and Production Lines Starting Operation (2017-2020)



Semiconductor Industry Development

Industry Center Shifts Through the Decades

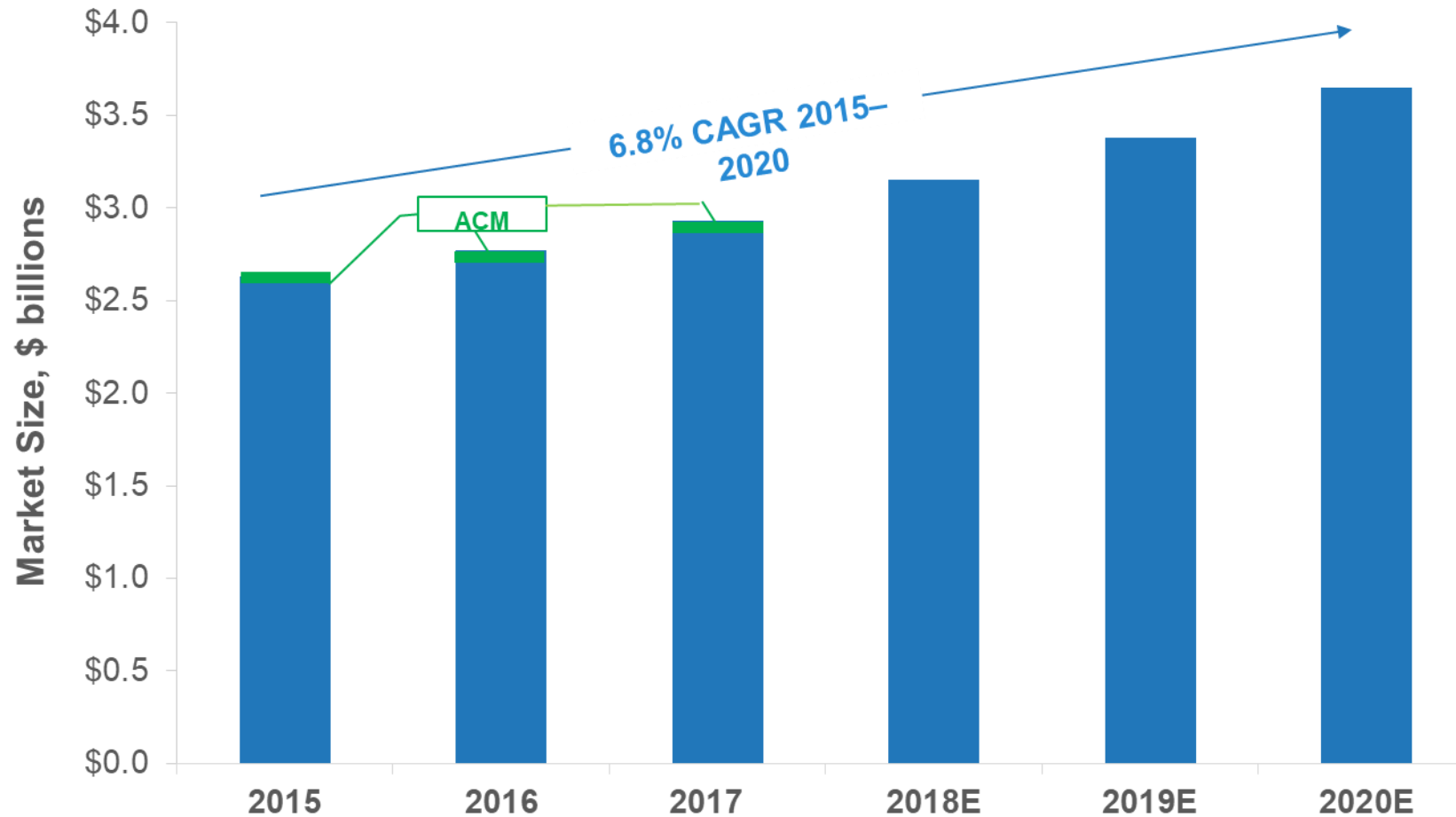


Strong presence in Asia and *close proximity* to Chinese customers is key competitive advantage

Source: World Fab Forecast Report (November 2016, SEMI)

ACM's opportunity increases as industry moves to advanced processes

Projected Market Growth 6.8% Annually 2015-2020



Growth Drivers:

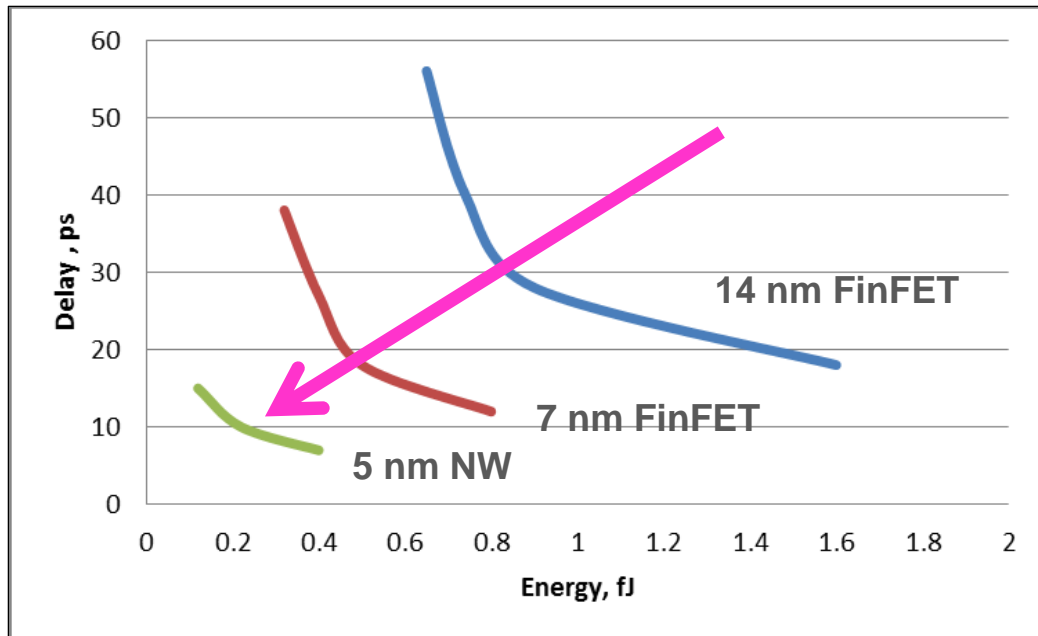
1. Ramp of current customers
2. Penetration of additional cleaning steps
3. New Customers
4. New products

Source: Transparency Market Research Pvt. Ltd., Report – Global Semiconductor Wafer Cleaning Equipment Market, December 2016

Moore's Law Demands New Lithography & Cleaning Technologies

Device are Continually Driving to Smaller Nodes For:

1. Higher Performance
2. Greater Energy Efficiency
3. Lower Cost



Smaller Nodes Lead to Significant Manufacturing Challenges

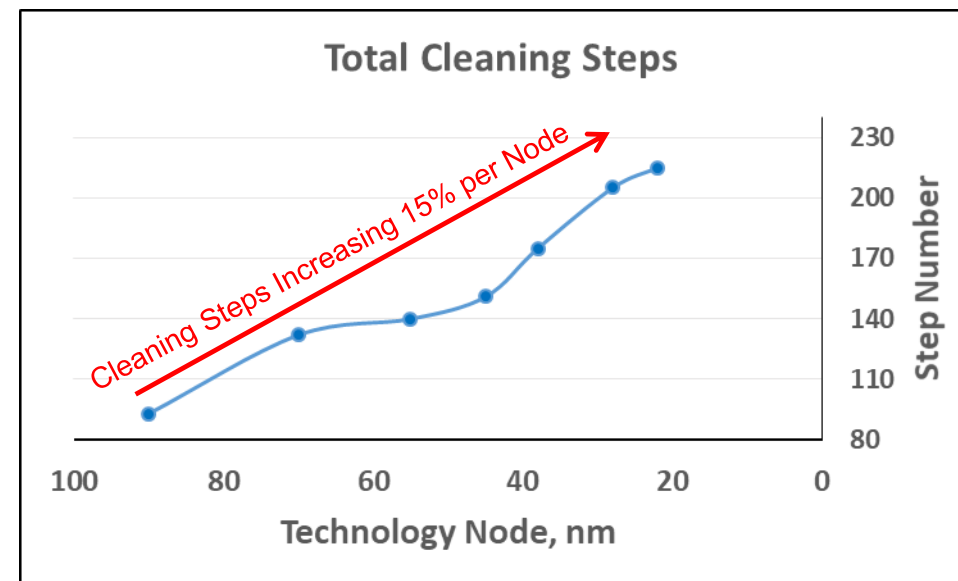
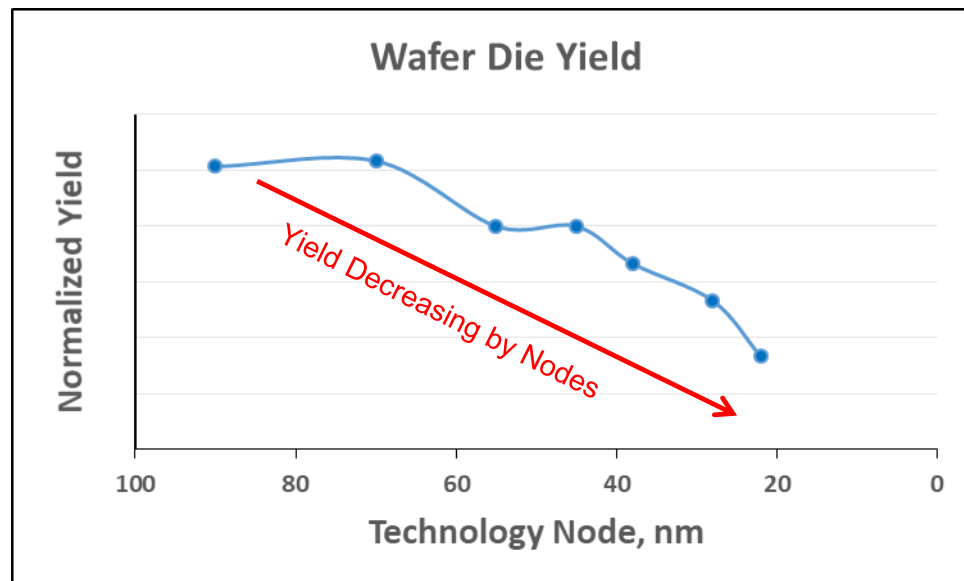
Key Process Equipment Groups

- Implantation
- Deposition
- **Microlithography**
- Etch
- **Clean**
- CMP
- Metrology

**Most Critical for
22nm and Smaller
Node Devices**

ACM offers wafer cleaning equipment designed to address one of the two major manufacturing challenges

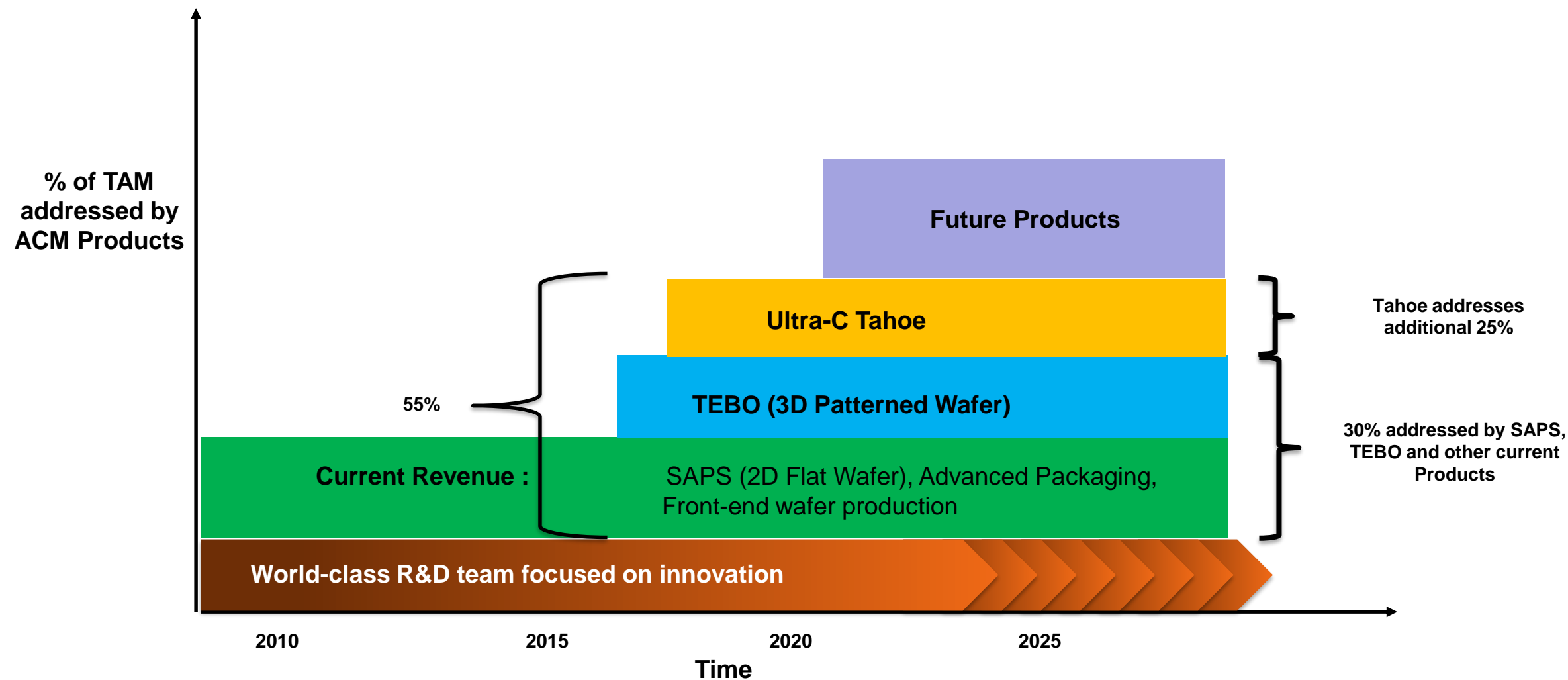
Semiconductor Yield Trend Challenges Profitability



** Both graphs are customer data

- We estimate that 1% yield loss can lead to annual profit decrease of **\$30M to \$50M**
 - The estimate is based on a DRAM fab with 100,000 wafer starts per month
 - The impact may be even greater for a fab making higher ASP logic chips
 - Moreover, a lower yield may require greater fab capacity and greater capital spending
- To remedy the problem, more cleaning steps with breakthrough capabilities are needed

Our Product Expansion Vision



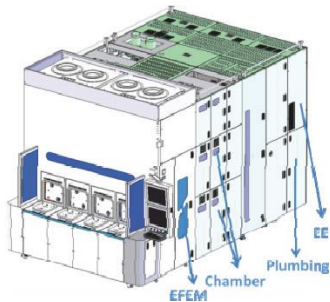
SAPS: Megasonic Cleaning for 2D Structures

Best-in-class yield improvements for 45nm and below

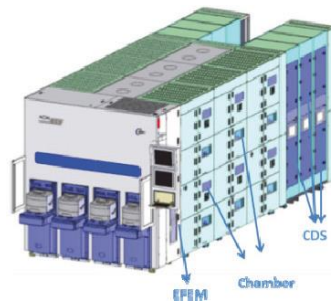
SAPS Tool



System Configurations



SAPS II, 8-chamber



SAPS V, 12-chamber

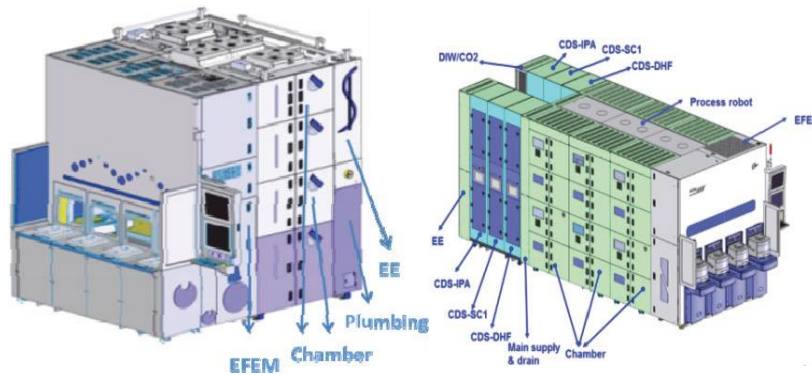
- ACM's main product line, majority of 2018 sales
- Designed for wafers with flat and simple patterned surfaces
- More than 40 tools in use at five major semiconductor manufacturers
- \$2.5-5.5 million ASP depending on configuration and feature options
- 22 patents covering ACM proprietary megasonic cleaning techniques

TEBO: Disruptive Solution for 3D Patterned Wafer Surface

TEBO Tool




System Configurations



TEBO II, 8-chamber

TEBO V, 12-chamber

- Patented solution removes defect particles in 3D structures/ FinFETs without damage
- First TEBO delivered to  in July 2017, also being evaluated by a selected group of leading memory and logic chip manufacturers
- \$3.5-6.5 million ASP depending on configuration
- Shipment ramp expected in late 2018 with revenue in 2H'2019 and beyond

Advanced Packaging Equipment

- Leverage our technology and extend applications to packaging factories in Asia, especially in China
- Focus on custom-made differentiated equipment with customer-requested features
- Products include scrubbers, coaters, developers, photoresist strippers, wet etchers, copper platters
- More than 42 tools shipped
- Expected tool ASP: \$500K-\$2M except copper platter
- Expected tool ASP for copper-plater: \$3+ M



Ultra ECP



- For application in Copper Bumper
- Incorporated proprietary plating technology with 16 plating chambers
- Reduce CoO for customers

Existing ACM Customer Single-Wafer Cleaning Tool Needs 2018-2019

- **ACM SAPS tool addressable market of existing customers with known fab ramps**
 - These customers already have SAPS tools qualified in production

Existing Customer	Application	# of Lines	Wafer Starts per Month Plan	Estimated Total Cleaning Tools 2018	Estimated Total Cleaning Tools 2019
A	DRAM	1	60K	48	58
B	Foundry	1	25K	33	30
C	Foundry	2	35K	25	73
D	3D NAND	1	60K	30	60
Total #		5	180K	136	221

- **Anticipated ACM cleaning tool additional addressable markets for 2018-2019:**
 - TEBO tool existing customers transitioning from engineering evaluation to production ramp
 - New customers adopting SAPS , TEBO and packaging tools such as copper-plater

Expanding Production Capacity to \$350 million per year

- Original factory delivers ~ \$100 million of annual capacity with 36,000 square feet of production floor
- New Factory adds \$250 million of annual production capacity with 50,000 square feet



20-minute drive from Shanghai HQ



\$1.5 million of Capex deployed in 1H'18



Initial production expected Q3 2018

ACM Management Team: Decades of Industry Experience



Name: David Wang, President and Chief Executive Officer
Degree: Ph.D. Osaka University; BSc Tsinghua University
Years of Exp: 25
Experience: Low-k electronics research director, Quester Tech.



Name: Lisa Feng, Chief Accounting Officer,
ACM Research (Shanghai), Inc.
Degree: Master degree of Accountancy
Years of Exp: 28
Experience: Corporate Controller at Amlogic Inc.



Name: Jian Wang
Vice President, Research and Development,
ACM Research (Shanghai), Inc..
Degree: MSc
Years of Exp: 15
Experience: ACM Research



Name: Mark McKechnie, Vice President, Finance
Degree: BSEE Purdue; MBA Kellogg/Northwestern
Years of Exp: 25
Experience: Motorola, Intel, Bank of America, Evercore



Name: Fuping Chen, Vice President, Sales
ACM Research (Shanghai), Inc..
Degree: MSc
Years of Exp: 12
Experience: Cleaning Manager at SK Hynix



Name: Sothera Cheav
Vice President, Manufacturing
ACM Research (Shanghai), Inc..
Degree: BSc
Years of Exp: 25
Experience: ACM Research

ACM Board and Advisory

Board of Directors

Average of 25+ Years Experience in Semiconductor Industry and High Tech Business



Dr. David H. Wang
ACM CEO & Founder



Dr. Haiping Dun
*Engineering Director at Intel;
CEO at Champion*



Prof. Chenming Hu
*Inventor of FinFET;
Professor at UC Berkeley*



Tracy Liu
*CPA, M.S. in
Accounting & Tax*



Yinan Xiang
*General Manger of
SSTVC*



Zhengfan Yang
*Director of
Sino IC*

Advisory Board

30+ Year Experience in Semiconductor Industry and High Tech Investment



Prof. Chenming Hu
*Inventor of FinFET;
Professor at UC Berkeley*



Lip Bu Tan
CEO at Cadence Design System



Dr. Stephen Chiao
*Professor at SJSU;
Sycamore Ventures*



Dr. Chiang Yuan Yang
*VP & GM
Intel Photomask Operation*



Prof. Srinu Raghavan
*Professor of MSE
at University of Arizona*

Q2 2018 Operating Highlights

- Record quarterly revenue, \$20.8 million, up 138% y/y
- Non-GAAP Operating Margin 12%
- Major new DRAM customer in China
- \$250M of additional annual capacity added with new factory
- Pipeline Remains Strong
- Raised 2018 Revenue Outlook to \$70 million

TECHNOLOGY DEEP DIVE

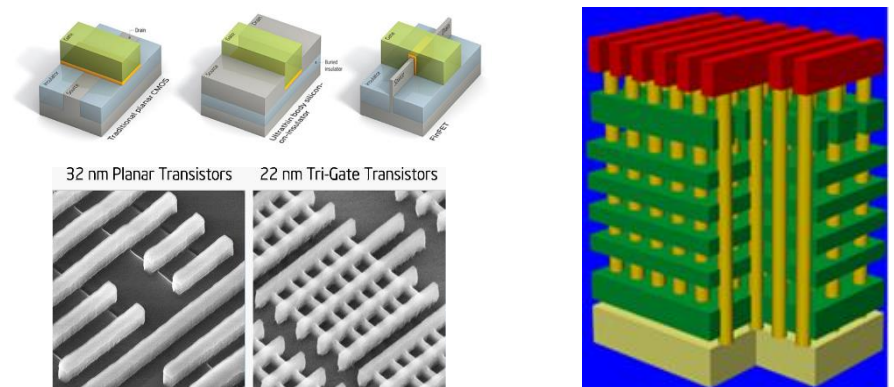
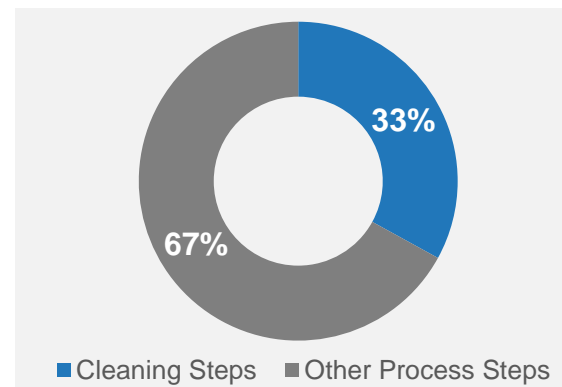
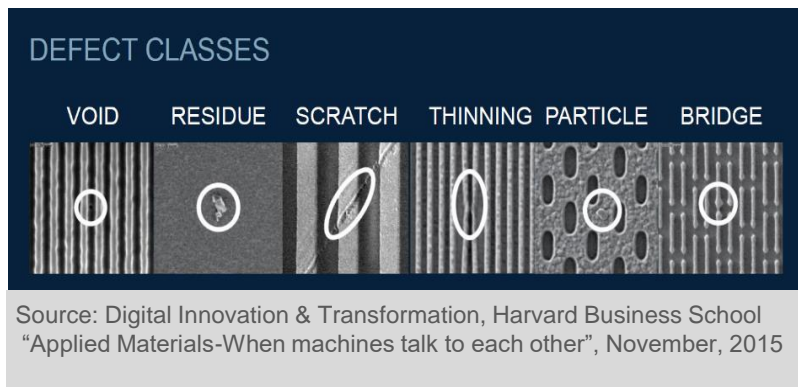
Importance and Challenges of Wafer Clean in Semiconductor Manufacturing

Importance of Wafer Cleaning

- Wafer cleaning is implemented to remove defects and particles in order to achieve good die yield
- More than 1/3 of process steps are cleaning steps
- 20 nm node DRAM: as many as 200 cleaning steps

Challenges for Advanced Technology Nodes

- New transistor architectures, ever smaller & fragile features, and 3-D structures lead to inadequacy or failure of conventional cleaning
- **“Killer Defect” sizes become smaller**
- **Poor PRE (Particle Removal Efficiency)**
- **Damage to fine device features**

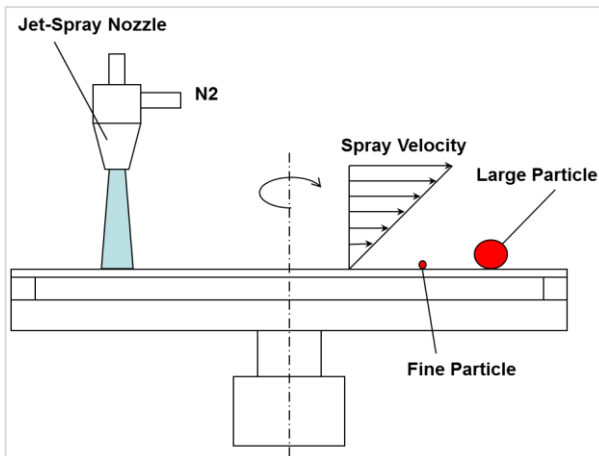


ACM's proprietary SAPS & TEBO solutions are designed to address these issues

SAPS: Breakthrough Use of Megasonic For Advanced Processes

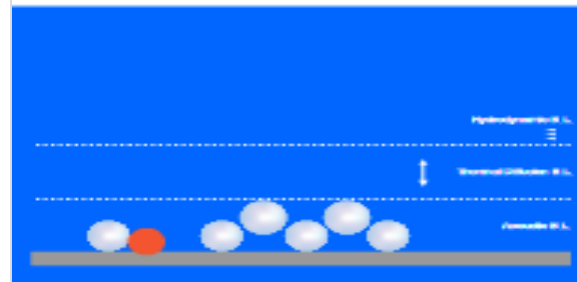
Conventional Jet-Spray

Ineffective at removing small defects at today's advanced nodes and geometries



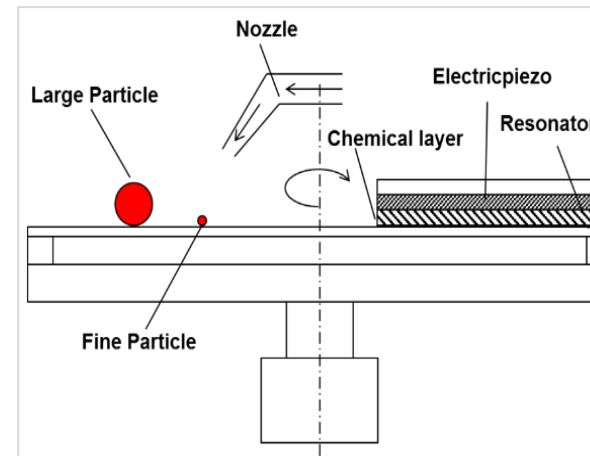
Megasonic Technology

High Frequency RF energy removes smallest particles through cavitation



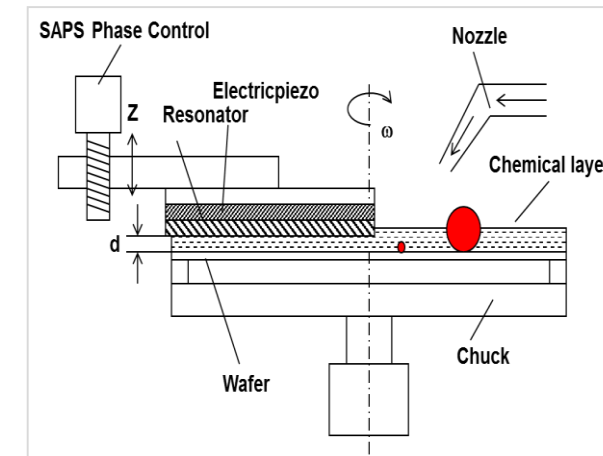
Early Megasonic Dead End

Abandoned by industry due to challenges at more advanced nodes and geometries

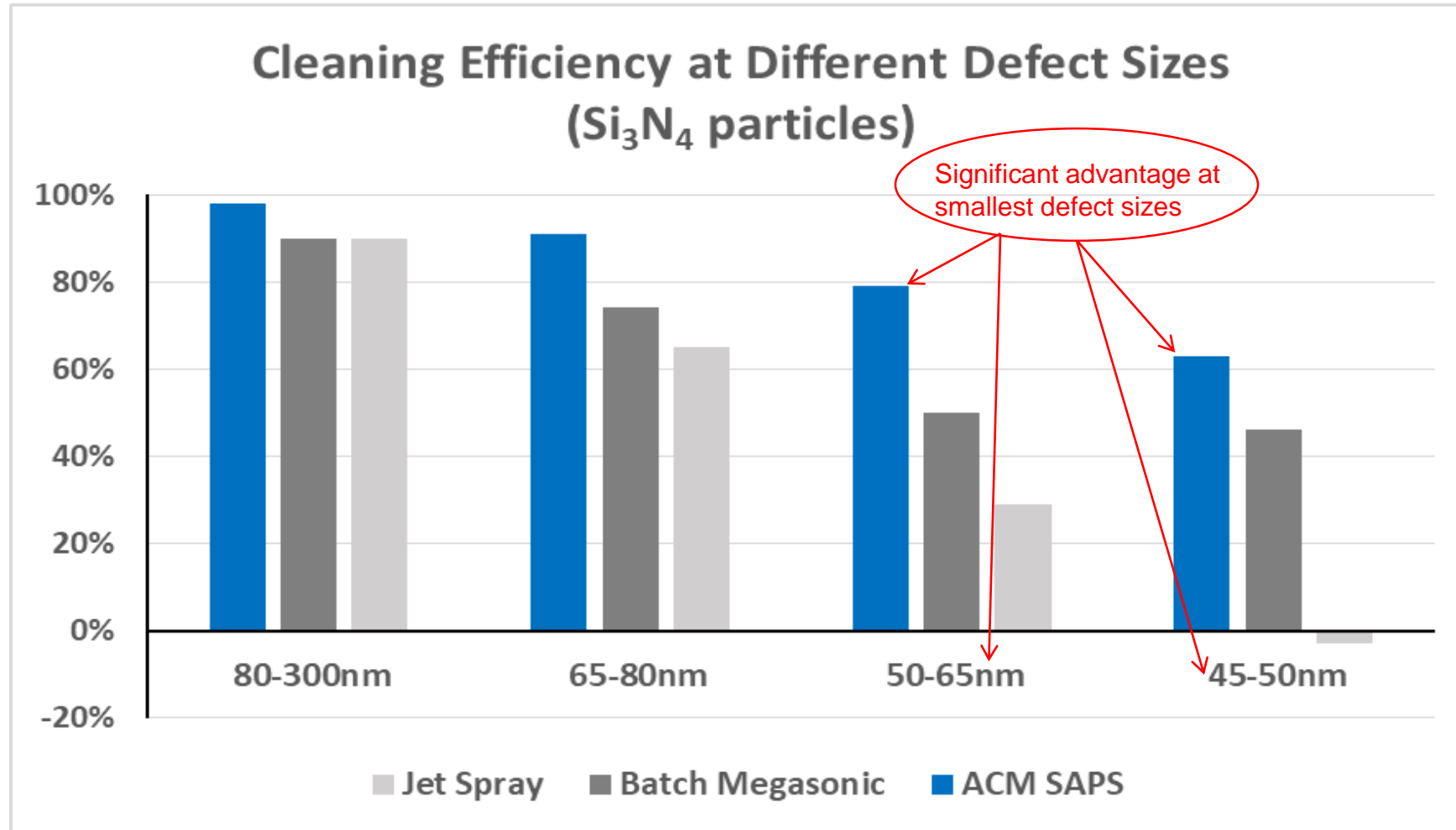


ACM SAPS – Uniform Energy

Best-in-class cleaning with increased advantages at 45 nm nodes and beyond



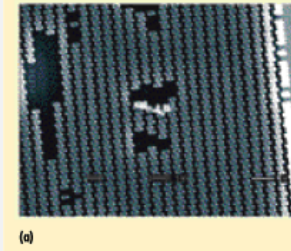
SAPS Efficiency is Consistently Better than Conventional Technologies



Source: ACM Research & Customer

TEBO: Proprietary Technology Reduces or Eliminates Feature Damage

As device features become *smaller and more fragile* with high aspect ratios (feature structure depth to width ratio), conventional cleaning processes can lead to damages and loss of yield



SEM images of damages at 50-nm DRAM storage capacitors following a dSC-1 clean with megasonics in a batch immersion tool using high power densities

Source: Micromagazine.fabtech, by John Rosato, et al., *SCP Global Technology*

Conventional Megasonic Cleaning



Transit cavitation results in violent micro-jet causing damage to wafer structures

TEBO Megasonic Cleaning

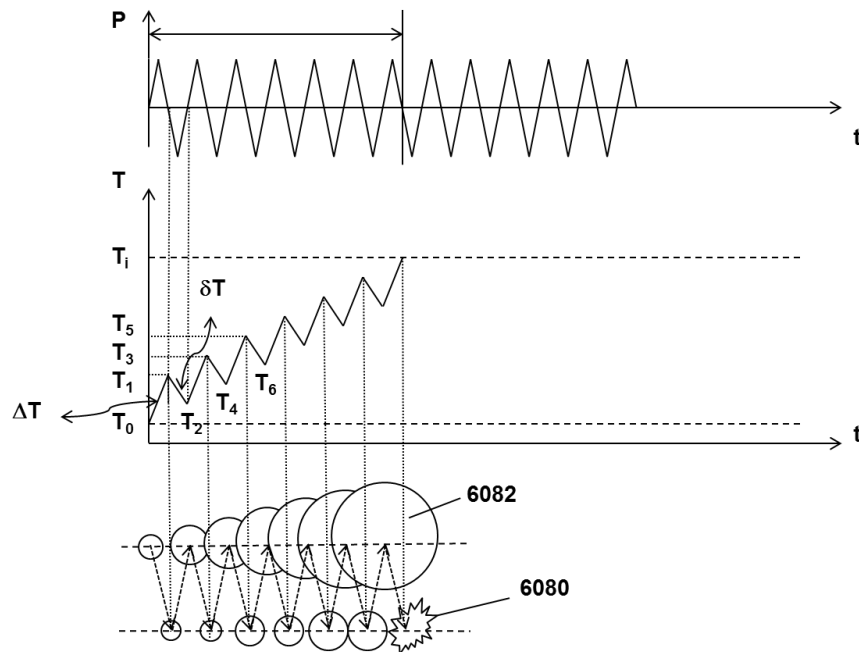


Stable cavitation

TEBO Technology: Works by Controlling Transit Cavitation Formation

Conventional Megasonic Cleaning

Transit Cavitation Implosion
Damages Wafer Structure



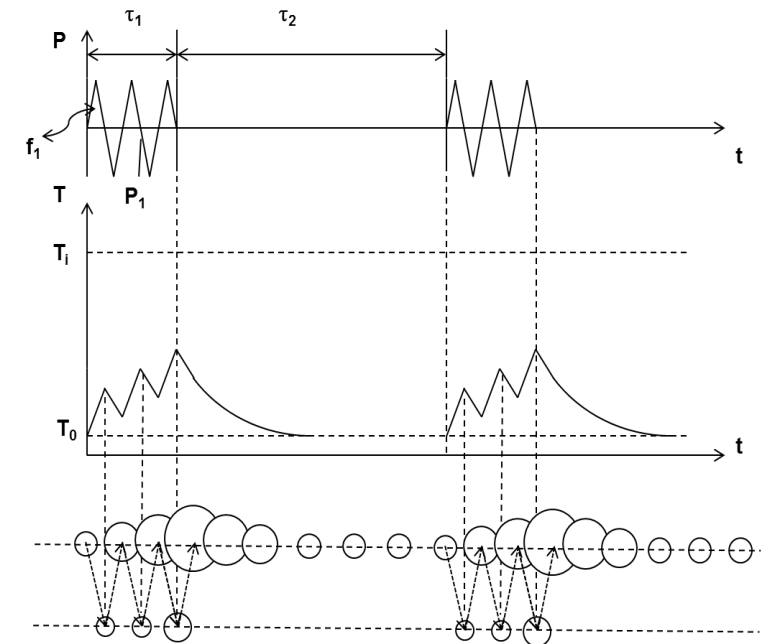
Megasonic
Energy
Cycles

Cavitation
Temperature

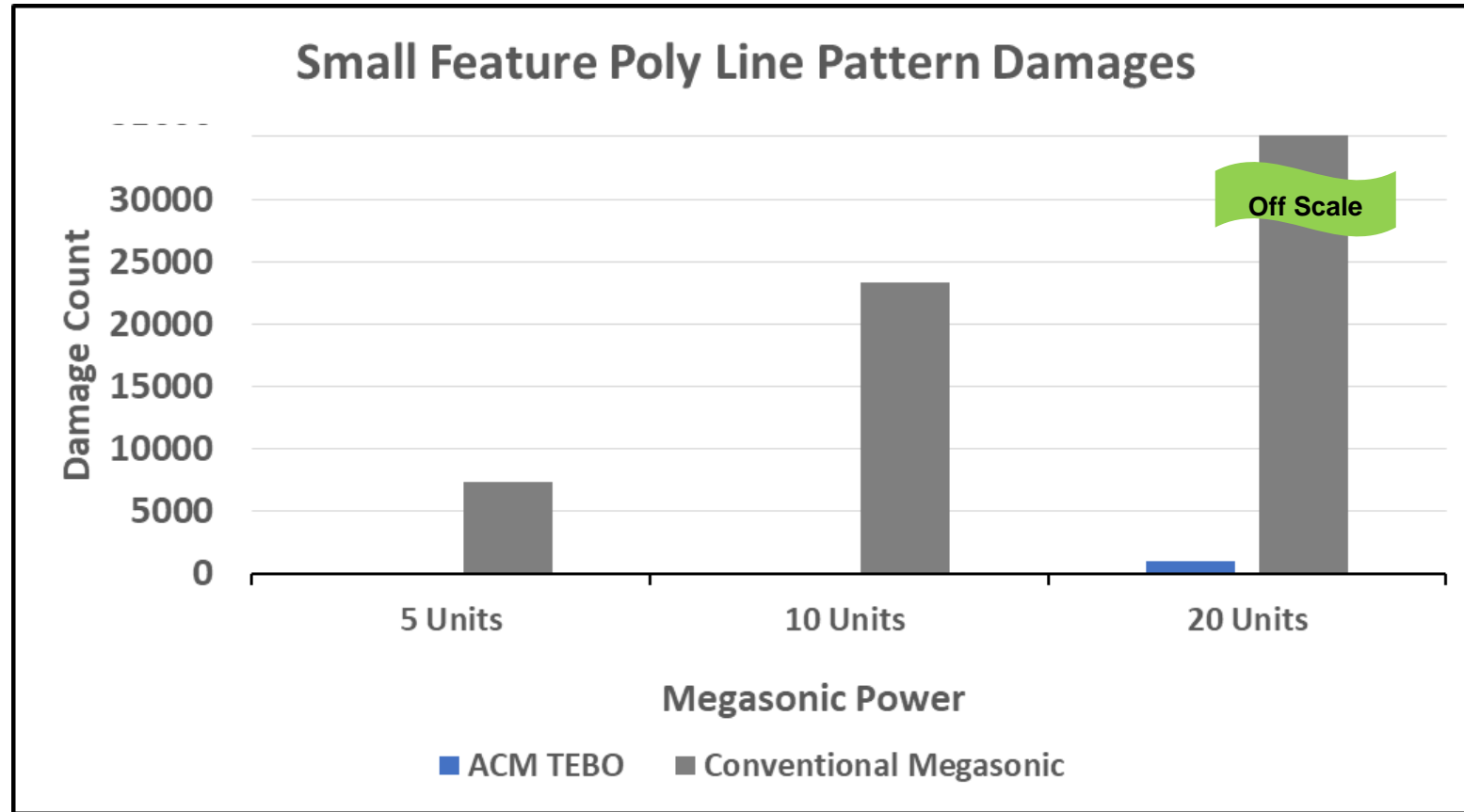
Cavitation
Size in
Oscillation

TEBO Megasonic Cleaning

Stable Cavitation, Effective Cleaning, Low/No
Damage



ACM TEBO vs. Conventional Megasonic on Pattern Damage Performance



- Adequate power level is needed to ensure effective cleaning action on the wafers
- However conventional mega-sonic clean at such power causes severe pattern damages
- TEBO can operate at such power with effective clean and no/low damages